Difference between 8085 and 8086 µP :-

	8085 µP	8086 µP
1.)	Data Bus is of 8 bits	Data Bus is of 16 bits.
2.)	Address Bus is of 16 bits	Address Bus is of 20 bits.
3.)	Memory capacity is 64 kB	Memory capacity is 1 MB.
4.)	The input / output port addresses are of 8 bits.	The input / output port addresses are of 8 bits.
5.)	The operating frequency is 3 MHz.	The operating frequency is 5 MHz, 8 MHz, 10 MHz.
6.)	8085 µP has single mode of operation.	8086 has 2 modes of operation: 1.) Minimum mode – single CPU processor 2.) Maximum mode – Multiple CPU processor.
7.)	It does not have multiplication and division instructions	It has multiplication and division instructions.
8.)	It does not support pipelining.	It supports pipelining.
9.)	It does not support instruction queue.	It supports instruction queue.
10.)	Memory space is not segmented.	Memory space is segmented.
11.)	It consists of 5 flags.	It consists of 9 flags.

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Characteristics of a μP :-

- **Instruction Set :-** Set of complete instructions that the μP executes, is termed as Instruction set.
- **Word Length :-** The no. of bits processed in a single instruction is called word length or word size. Greater the word size, larger the processing power of the CPU.
- **System clock speed :-** Clock speed determines how fast a single instruction can be executed in a processor. The μP's pace is controlled by the system clock.

Classification of Microprocessors :- Besides the classification based on word length, the classification is also based on the architecture i.e. instruction set of the μP. These are categorised into RISC and CISC.

① **RISC :-** It stands for Reduced Instruction Set Computer. It is a type of microprocessor architecture that uses a small set of instructions of uniform length. These are simple instructions which are generally executed in one clock cycle.
Eg.- SPARC, POWER PC etc.

② **CISC :-** It stands for Complex Instruction Set Computer. These processors offer the users, hundreds of instrs. of variable sizes. CISC architecture includes a complete set of special purpose circuits that carry out these instructions at a very high speed.
Eg. - Intel Architecture, AMD

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③ EPIC: It stands for Explicitly Parallel Instruction Computing.

The best features of RISC and CISC processors are combined in the architecture. It implements parallel processing of instructions rather than using fixed length insts. The working of EPIC processors are supported by using a set of complex instructions that contain both basic instructions as well as the information of execution of parallel instructions.

Diff b/w CISC and RISC

CISC	RISC
* A large no. of instructions are present in the architecture.	Very fewer insts. are present. The no. of insts. are generally less than 100.
* Some insts. with long execution times. These include instructions that copy an entire block from one part of memory to another and others that copy multiple registers to and from memory.	No inst. with a long execution time due to very simple inst. set.
* Variable length encodings of the instructions.	Fixed-length encodings of the instructions are used.
* CISC supports array.	RISC doesn't support array.
* Condition codes are used.	No condition codes are used.

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Type of Segmentation :-

① Overlapping Segment :- A segment starts at a particular address and its maximum size can go upto 64kB. But if another segment starts along with this 64kB location of the first segment, then the two are said to be Overlapping Segment.

② Non Overlapped Segment :- A segment starts at a particular address and its maximum size can go upto 64kB. But if another segment starts before this 64kB location of the first segment, then the 2 segments are said to be Non overlapped segment.

Rules of Segmentation :-

a.) The starting address of a segment should be such that it can be evenly divided by 16.

b.) Minimum size of a segment can be 16B and the maximum can be 64kB.

Segment	Offset Registers	Function
CS	IP	Address of next instruction
DS	BX, DI, SI	Address of data
SS	SP, BP	Adress in the stack
ES	BX, DI, SI	Address of destination data (for string operations)

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Advantages of Segmentation:-

* It provides a powerful memory management mechanism.
* Data related or stack related operations are performed in diff. segments.
* Code related operation can be done in separate code segments.
* It allows to easily processes to share data easily.
* It allows to extend the address ability of the processor, i.e. segmentation allows the use of 16 bit registers to give an addressing capability of 1 MB. Without segmentation, it would require 20 bit registers.
* It is possible to enhance the memory size of code data or stack segments beyond 64 kB by allotting more than one segment for each area.

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